Return Link Processing PCI Card Critical Hardware Design Review

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November 21, 1996

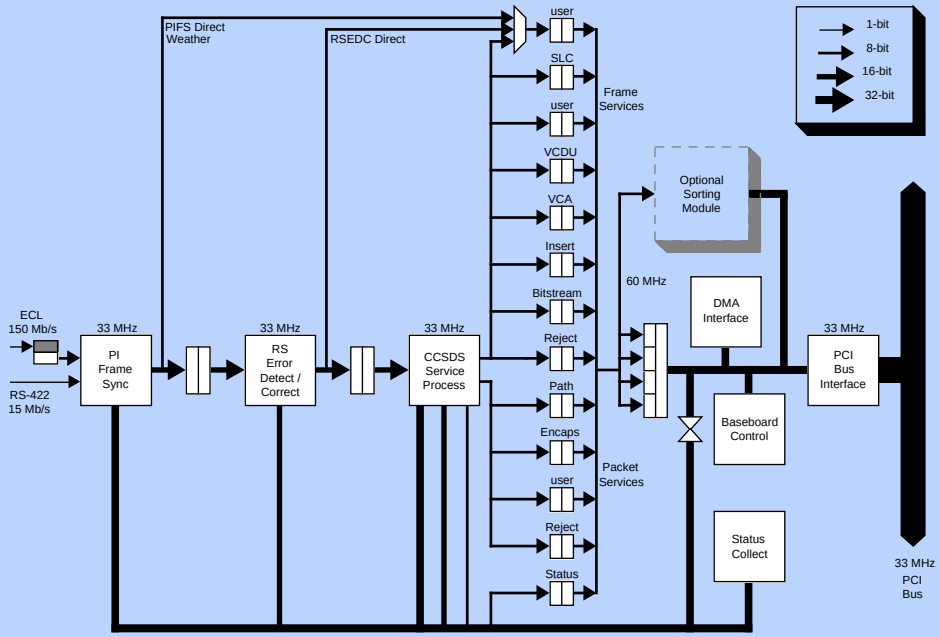
Presentation Overview

- Goals
- Architecture
- Functional Elements
- Optional Sorting Module
- Software Interface
- Verification
- Replication Cost
- PDR Issues
- Schedule

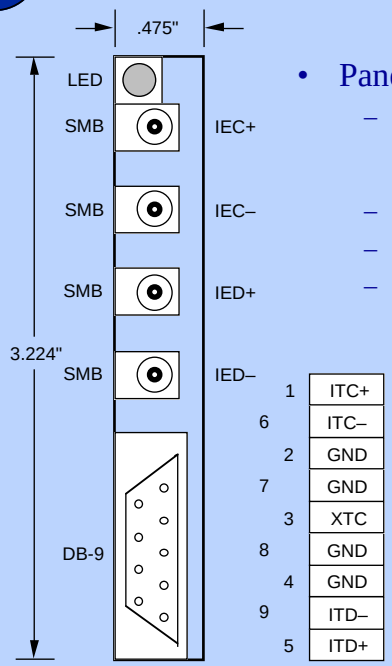
Goals

- Single-card "return link" data processing solution
  - telemetry frame synchronization & CRC/BTD decoding
  - Reed-Solomon error detection/correction
  - CCSDS AOS Service/Conventional Packet & Frame processing
  - optional additional processing
- Support various telemetry forms
  - real-time CCSDS data
  - weather satellite data
- Support popular host platforms
  - IBM PC-compatible to 50 Mb/s
  - Apple Macintosh-compatible to 50 Mb/s
  - Sun SPARCstation to 150 Mb/s
  - DECstation to 150 Mb/s
- Facilitate level-0 processing
- Low replication cost, multiple price/performance points

Architecture



Functional Elements



1	ITC+
6	ITC–
2	GND
7	GND
3	XTC
8	GND
4	GND
9	ITD–
5	ITD+

- Panel I/O
  - ECL clock & data: 150 Mb/s nominal, 267 Mb/s maximum @ 33 MHz (up to 400 Mb/s @ 50 MHz)
  - RS-485/422 clock & data: 10 Mb/s nominal
  - external 10 MHz TTL timecode reference signal
  - software-controlled LED

Functional Elements, cont'd

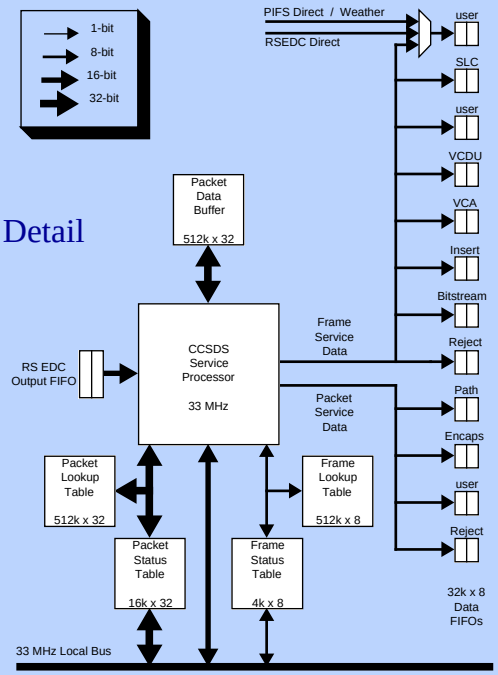
- Code 521 Parallel, Integrated Frame Synchronization ASIC
  - bit-parallel byte-serial data from ECL serial-to-parallel converter, differential or single-ended selectable through Baseboard Control
  - bit-serial data from RS-485/422 buffer
  - 33 MHz processing clock
  - outputs 8- or 16-bit data at up to the processing clock rate (33 MHz)
  - outputs to Code 521 Reed-Solomon Error Detection/Correction ASIC or Data FIFO, selectable through Baseboard Control, useful for Weather data
  - 10 MHz timecode reference clock from either local oscillator or external source, selectable through Baseboard Control
  - uses PIFS internal CCSDS Day Segmented time code format
  - accepts data input through CPU interface (PCI bus), useful for Internet Protocol (future NASCOM) data or testing
  - has 32, 32-bit registers for control & status
  - JTAG, accessable through PCI bus

Functional Elements, cont'd

- Code 521 Reed-Solomon Error Detection/Correction ASIC
  - 33 MHz processing clock
  - inputs and outputs 16-bit data at up to half the processing clock rate (16.7 MHz)
  - outputs data to CCSDS Service Processing IC or data FIFO, selectable from Baseboard Control, useful for testing
  - has 40, 16-bit registers for control & status (on 32-bit boundaries)

Functional Elements, cont'd

CCSDS Service Processor Detail



Functional Elements, cont'd

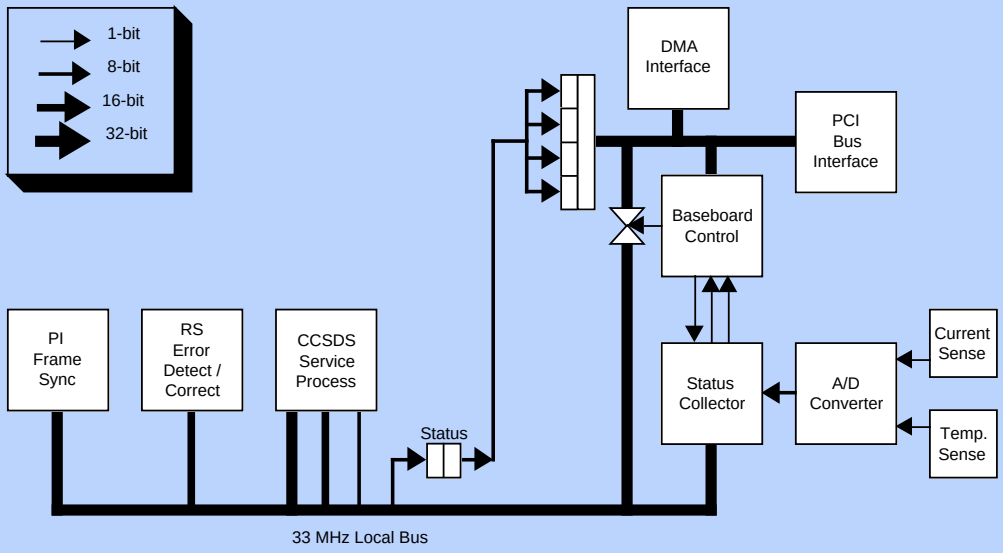
- Code 521 CCSDS Conventional Packet/AOS Service Processing ASIC
  - 33 MHz processing clock
  - inputs 8- or 16-bit data at up to half the processing clock rate (16.7 MHz)
  - outputs 8-bit data at the processing clock rate (33 MHz) to up to 4 packet and 8 frame service ports concurrently
  - 512 kB frame lookup table memory
  - 2 MB packet lookup table memory
  - 4 kB frame status dual-ported memory
  - 64 kB packet status dual-ported memory
  - 2 MB packet buffer memory
    - » 128 virtual channels with 8 KB maximum packet length
    - » 16 virtual channels with 64 KB maximum packet length

Functional Elements, cont'd

- SP, cont'd
  - each service port connected to a 32 kB Data FIFO, so for 16 kB transfer block size, get:
    - » 13.1 ms buffer @ 10 Mb/s
    - » 2.62 ms buffer @ 50 Mb/s
    - » .874 ms buffer @ 150 Mb/s
  - highest data multiplication expected: 3x ⇒ 450 Mb/s output
  - has 112, 16-bit registers for control & status (on 32-bit boundaries)
  - JTAG, accessible through PCI bus

Functional Elements, cont'd

Status Collector Detail



Functional Elements, cont'd

- Status Collector CPLD
  - 33 MHz local bus clock
  - has 2, 32-bit registers
  - collects status from other devices on the board and places it into a Data FIFO
    - » Status Request register takes a code indicating which status to collect:
      - PIFS registers, 128 B
      - RS registers, 80 B
      - SP registers, 224 B
      - SP frame status, up to full 4 kB in 16-B chunks
      - SP packet status, up to full 64 kB in 4-B chunks
    - » host write to Status Request register immediately writes Status Collector register values (8 B) to Data FIFO and then commences collecting requested status
    - » when Status Request fulfilled, asserts Status Done signal which is indicated in a Baseboard Condition register and/or causes the generation of an interrupt
  - periodically and automatically reads the Analog-to-Digital Converter and holds the values in the ADC register
    - » 8-bit code for current draw through 5V bus (power)
    - » 8-bit code for ambient temperature

Functional Elements, cont'd

- SC, cont'd
  - "detachable" local bus keeps status collection traffic from interfering with telemetry data flow
  - decodes device addresses on its portion of the local bus, arbitrates with Baseboard Controller to "attach" local busses when a PCI access falls within its space
  - AMD MACH 465, 12 ns
    - » 10,000 gates, 80% utilization
    - » 146 pins, 53% utilization
  - in-circuit reprogrammable through JTAG port, accessible via on-board MACHPRO connector

Functional Elements, cont'd

- DMA Interface CPLD
  - has 5, 32-bit registers for control & status
  - controls data flow from 8-bit Data FIFOs to 32-bit Transfer FIFO
    - » sustains 1 byte per 60 MHz clock cycle (480 Mb/s) during a Byte Transfer
    - » Transfer Request register takes number of bytes and selection code for Data FIFO
    - » if Data FIFO goes empty before end of Byte Transfer, remainder of Byte Transfer is filled, and counted in the Fill Count register
    - » dual Byte Transfer channels (two pairs of Transfer Request & Fill Count registers) facilitates pipelining of the two PCI Bridge Chip DMA engines
    - » host can select byte ordering and reset the Transfer FIFO through a Control Register
  - 128 kB Transfer FIFO maximizes PCI bus utilization with large bursts
  - controls data flow from 32-bit Transfer FIFO to PCI Bridge Chip
    - » DMA bursts at 1 longword per 33 MHz clock cycle (1 Gb/s)
    - » host programs the Transfer FIFO Almost-Empty Flag, and PBC DMA-reads are held off until flag clears or Byte Transfer ends, to generate long fast PCI burst
    - » if DMA empties the Transfer FIFO before the Byte Transfer completed, PBC DMA is once again held off to save up for another burst

Functional Elements, cont'd

- DMA Interface CPLD, cont'd
  - provides facilities for the host to write directly to the Transfer FIFO and read directly from the Data FIFOs for testing and flushing
  - end-of-session flush is performed by transferring entire Data FIFO space and observing the Fill Count registers
  - AMD MACH 465, 12 ns
    - » 10,000 gates, 82% utilization
    - » 146 pins, 74% utilization
  - in-circuit reprogrammable through JTAG port, accessible via on-board MACHPRO connector

Functional Elements, cont'd

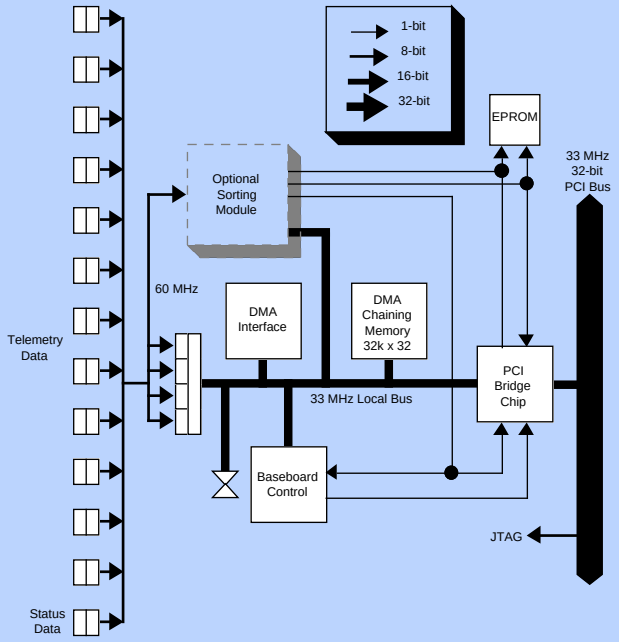
- Baseboard Control CPLD
  - 33 MHz local bus clock
  - has 5, 32-bit registers
  - inputs, registers, & masks all interrupt sources & generates interrupt
    - » 53 interrupt sources indicated in 2 Condition registers
      - as many FIFO flags as permitted by available pins
      - foremost FIFO overflow condition latched and clearable
      - status collection fulfilled condition
    - » all 53 interrupt sources are individually maskable in 2 Mask registers
    - » interrupt itself can also be disabled
  - baseboard control functions collected into single Control register
    - » LED toggle
    - » differential or single-ended ECL input select
    - » SP, PIFS-Direct, or RS-Direct data routing mode select
    - » on-board or off-board PIFS timecode reference clock select
    - » universal FIFO flag programming signal
    - » 16 individual reset signals
    - » interrupt source indication mode, raw or masked

Functional Elements, cont'd

- Baseboard Controller CPLD, cont'd
  - "detachable" local bus keeps status collection traffic from interfering with telemetry data transfer
  - decodes space addresses, arbitrates with Status Collector to "attach" local busses when such a PCI access occurs, controls bus switch
  - decodes DMA-Chaining Memory addresses
  - AMD MACH 465, 12 ns
    - » 10,000 gates, 53% utilization
    - » 146 pins, 97% utilization
  - in-circuit reprogrammable through JTAG port, accessible via on-board MACHPRO connector

Functional Elements, cont'd

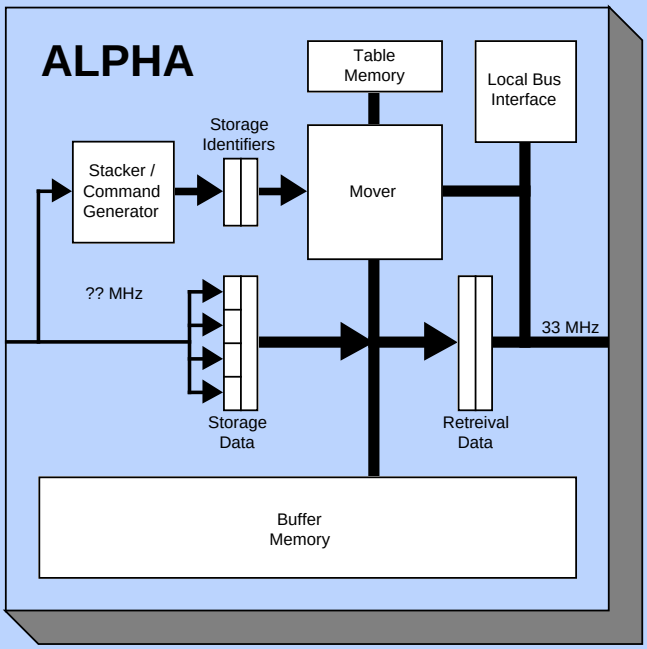
PCI Interface & Optional Sorting Module Connector Detail



Functional Elements, cont'd

- PCI Bus interface
  - V3 Corporation V962PBC i960Cx Local Bus / PCI Bus Bridge IC
    - » 33 MHz local and PCI bus clock inputs
    - » 1 Gb/s sustained throughput
    - » 32-bit demultiplexed address and data busses
    - » dual, chainable DMA engines (chaining available March 1997)
    - » two interrupt inputs used: Baseboard & OSM
    - » configuration read automatically from serial-EEPROM
    - » configuration EEPROM in-circuit reprogrammable
  - 32 k x 32-bit DMA-chaining / user memory

Optional Sorting Module



Optional Sorting Module, cont'd

- Major goals
  - increase sustained throughput (A)
  - reduce host CPU processing burden (A)
  - reduce post-processing requirements (A)
  - maximize PCI and local bus utilization (A)
- Examples of additional functionality
  - upgraded/custom buffering (A)
  - upgraded/custom sorting (A)
  - CCSDS Packet Segment reassembly
  - custom annotation formats
  - direct data output interface
  - data processing
  - automated board testing
  - automated board setup/control
  - PCI bus mastering
  - CPU

Optional Sorting Module, cont'd

- OSM Connector
  - to replace baseboard DMAI and Transfer FIFO functionality
  - to have both local bus slave and master capability
  - will be accessible from baseboard MACHPRO JTAG connector
  - will replace baseboard PBC Configuration EEPROM
  - can generate interrupt to both Baseboard Controller and PBC
  - single 200-pin connector for minimum impact on baseboard and mezzanine layout

Software Interface

- PCI Configuration
  - PBC autoconfigures itself from the on-board EPROM at powerup
  - OS or driver reads configuration data from PBC registers
- Setup
  - host writes into chip setup registers/memories: PBC, PIFS, RS, SP, BC
  - host programs Data FIFO amost-full and almost-empty flags through the SP
  - host programs Transfer FIFO almost-empty flag through the DMAI

Software Interface, cont'd

- Data transfer: event-driven host-initiated DMA to host memory
  - while no DMA:
    - » initiate one Status Collection
    - » modify interrupt masks
    - » turn on/off LED
    - » wait for Data FIFO Service interrupt
    - » poll board status
    - » initiate one or two Data FIFO Byte Transfers
    - » initiate one chained or atomic DMA
  - while DMA:
    - » wait for DMA Done interrupt
    - » perform other host processing
  - end-of-session flush:
    - » wait for no more interrupts
    - » check board status
    - » initiate one or two Data FIFO Byte Transfers
    - » initiate one or two chained or atomic DMAs
    - » check Fill Count registers
    - » extract incomplete data units from SP

Software Interface, cont'd

- Performance Tuning
  - flexible Data FIFO service block size: interrupts generated from programmable almost-full & almost-empty flags
  - flexible DMA burst size: holdoff generated from Transfer FIFO programmable almost-empty flag
  - software prioritizes Data FIFO servicing
  - software initiates collection and transfer of status data separately
- Test Points
  - most useful signals are conveniently accessed through the OSM connector
  - remaining useful signals occupy a small number of testpoints

Verification

- Verified interconnection, function, timing:
  - ECL input interface
  - DMA interface
  - status collection
  - baseboard control
  - bus switching
- Not Verifying:
  - PIFS IC & FIFO
  - RS IC & FIFO
  - SP IC & memories
  - PBC & EPROM

Replication Cost

PCB	$	500
ECL logic + power	$	140
PIFS ASIC	$	50
RS EDC ASIC	$	500
SP ASIC	$	190
10 SRAMs @ $128 ea.	$	1280
3 DPRs @ $56 ea.	$	170
19 FIFOs @ $93 ea.	$	1770
3 CPLDs @ $200 ea.	$	600
PCI Bridge IC	$	50
Remaining	$	500
Total	$	5750

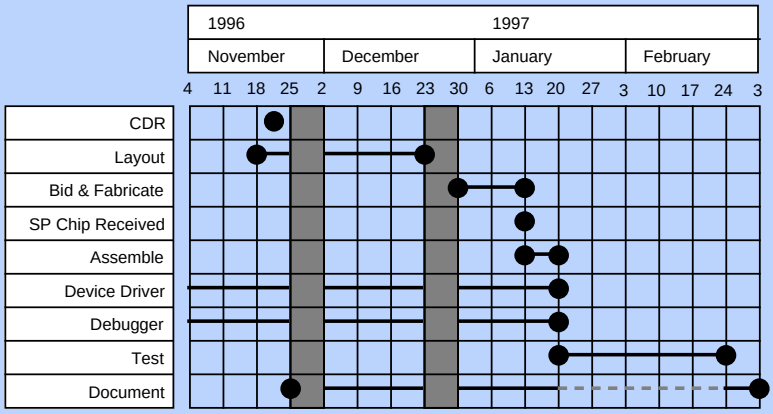
PDR Issues

- Eliminate some SP services: insignificant benefit
- Sorting module is required: architected
- DB9 connector safety: no active power
- SMA connectors too close: used SMBs
- Heat considerations: no CPU, low 33 MHz ok
- Layout fit to board: room to spare
- Software vs. hardware sorting on DEC Alpha: under investigation
- Mezzanine height: ok with careful layout
- Rough HDD: done
- Cost estimate: <$6k

PDR Issues, cont'd

- Power estimate:
  - PCI specs 5A @ 5V, 7.6A @ 3.3V per slot

	Theoretical Maximum	Theoretical Typical	Expectation
PCI10FR	6.5	5.6	2.4 -- measured
RLP	9.5	7.0	3.6 -- extrapolated from PCI10FR typical 4.2 -- extrapolated from PCI10FR maximum

  - excellent probability of success
    - » not possible for each device to draw stated power at the same time
      - can only access one device/bank from the data bus at a time
      - can only read one and write one FIFO at 60 MHz at a time
    - » unlikely that all other PCI slots will use their full 5A
  - other possibilities for investigation:
    - » DC/DC converters using 3.3V
    - » high-power PCI platforms
    - » external supply
    - » split design into multiple cards
  - power must be considered in OSM design

Schedule